REMARKS/ARGUMENTS

Claims 1-11 are pending in the application. By this amendment, claims 1, 2, 4 and 7 are being amended. No new matter is involved.

In Paragraph 1 on page 2 of the Office Action, claim 4 is objected to because the recitation "first signal" in the last line thereof is incorrect and should be changed to the second signal. In response, Applicant is amending claim 4 to recite the second signal in the last line thereof. Therefore, claim 4 as so amended should now be clear and definite.

In Paragraph 3 on page 2 of the Office Action, claims 1, 2, 3 and 4 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,383,205 of Makihara, et al. Thereafter, claims 5-11 are rejected under 35 U.S.C. § 103(a) based on various combinations of Makihara with U.S. Patent 4,077,565 of Nibby, Jr., et al., U.S. Patent 6,618,450 of Hatta, U.S. Patent 5,095,417 of Hagiwara, et al., and U.S. Patent 5,737,022 of Yamaguchi, et al. These rejections are respectfully traversed.

Claim 1 defines an error detection and correction circuit which includes a selection circuit, an error detection and correction unit and a switch circuit. As amended herein, claim 1 further defines the error detection and correction circuit thereof in terms of "a memory", and "wherein the selection circuit selects the second signal and sends the second signal to the memory", "the memory stores the second signal until an amount of the stored second signal becomes a predetermined amount", and "the error detection and correction unit receives the predetermined amount of the second signal when the amount of the second signal in the memory becomes the predetermined amount".

U.S. Patent 5,383,205 of Makihara describes a semiconductor memory device having an error correction circuit and an error correction method of data in a

semiconductor memory device. However, Makihara, et al. does not show or suggest the features in accordance with the present invention as added to claim 1 as amended. More specifically, the reference does not show or suggest in combination a memory, a selection circuit selecting the second signal and sending the second signal to the memory, the memory storing the second signal until an amount of the stored second signal becomes a predetermined amount, and an error detection and correction unit receiving the predetermined amount of second signal when the amount of the second signal in the memory becomes the predetermined amount. Therefore, claim 1 as amended is submitted to clearly distinguish patentably over such reference.

Similar comments apply to claims 2, 3 and 4 which depend from and contain all of the limitations of claim 1. Claim 2 is being amended to correspond to claim 1 as amended herein. Therefore, claims 2-4 are also submitted to clearly distinguish patentably over Makihara, et al.

Regarding the rejection of claims 5 and 6 as unpatentable over Makihara in view of Nibby, Jr. '565 and Hatta '450, respectively, such claims depend from and contain all of the limitations of claim 1. Therefore, the attempted addition of Nibby, Jr. and Hatta to the combination of references does not cure the basic deficiency of Makihara with respect to claim 1. Such claims are also submitted to clearly distinguish patentably over the art.

Claim 7 is being amended by adding the limitations of claim 1 thereto. As so amended, claim 7 defines an error detection and correction circuit which includes a selection circuit, an error detection and correction unit and a switch circuit. The error detection and correction circuit is further defined in terms of "the error detection and correction signal sets a completion flag upon completion of error detection and correction with respect to the first signal received", and "the selection

circuit supplies the second signal to the error detection and correction unit when the selection circuit receives the second signal and detects the completion flag". As so amended, claim 7 is submitted to clearly distinguish patentably over the cited references. Makihara does not disclose or suggest a completion flag as recited in claim 7. Yamaguchi is concerned with a communication system for a motion picture image transmission apparatus. The function of the completion flag of Yamaguchi is different from that in accordance with the invention, as recited in claim 7. Therefore, claim 7 is submitted to clearly distinguish patentably over the art.

Claims 8-11 depend, directly or indirectly, from claim 7 and contain all of the limitations thereof. Therefore, such claims are also submitted to clearly distinguish patentably over the art.

In conclusion, claims 1-11 are submitted to clearly distinguish patentably over the prior art for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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Date: May 17, 2004

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